UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,742	03/12/2004	Richard Parent	CD03011	9219

7590 05/10/2005

Bradley T. Sako
WALKER & SAKO, LLP
Suite 235
300 South First Street
San Jose, CA 95113

EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,742	PARENT ET AL.	
	Examiner	Art Unit	
	Son L. Mai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-8 and 14-20* is/are allowed.

6)☒ Claim(s) *9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-12-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 03-12-04 has been considered.

Drawings

2. The drawings are objected to because the reference "flatch" in figure 3 should read –latch--. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 9, 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Furutani (U.S. Patent 5,673,231).

Regarding claim 9, Furutani teaches a method of reducing a standby current contribution in conductive lines of a memory device, comprising the steps of: providing at least one transistor (transistor 19 in figure 1) between each of a plurality of conductive lines (BL1a) arranged in a first direction within a memory cell array and a corresponding circuit (amplifier 5) coupled to the conductive line; programming a fuse-type element (fuse 9) to generate a control signal first value (signal Y1 is brought to low level) if an associated conductive line is determined to have a defect, and disabling each transistor when the associated control signal has the first value to prevent defect induced current from flowing through the transistor with respect to the corresponding conductive line.

Regarding claim 11, Furutani shows in figure 1, the at least one transistor (transistor 19) is between a bitline (BL1a) and a sense amplifier (5).

Regarding claim 12, even though not shown in figure 1, an equalization circuit is included in the sense amplifier circuit 5 as a means to equalize the data line pair I/O before reading data from memory array cells.

5. Claims 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamauchi et al. (U.S. Patent 6,246,627).

Regarding claim 9, Yamauchi teaches a method of reducing a standby current contribution in conductive lines of a memory device, comprising the steps of: providing at least one transistor (transistor 21 in figure 2B) between each of a plurality of conductive lines (8c) arranged in a first direction within a memory cell array and a corresponding circuit (power source 90) coupled to the conductive line; programming a fuse-type element (22) to generate a control signal first value (signal from element 22 is brought to low level) if an associated conductive line is determined to have a defect, and disabling each transistor when the associated control signal has the first value to prevent defect induced current from flowing through the transistor with respect to the corresponding conductive line.

Regarding claim 10, Yamauchi teaches at column 1, lines 38-64, the programming element is performed in a wafer test procedure.

6. Claims 9 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawai et al. (U.S. Patent 5,146,429).

Regarding claim 9, Kawai teaches a method of reducing a standby current contribution in conductive lines of a memory device, comprising the steps of: providing at least one transistor (transistor N in figure 5) between each of a plurality of conductive lines (R1) arranged in a first direction within a memory cell array and a corresponding circuit (ROW DECODER 3) coupled to the conductive line; programming a fuse-type element (fuse f1) to generate a control signal first value (signal to the gate of the transistor N is brought to low level) if an associated conductive line is determined to have a defect, and disabling each transistor when the associated control signal has the

first value to prevent defect induced current from flowing through the transistor with respect to the corresponding conductive line.

Regarding claim 13, Kawai also teaches that the at least one transistor is located between a wordline (R1) and a corresponding wordline driver circuit (included in ROW DECODER 3).

Allowable Subject Matter

7. Claims 1-8 and 14-20 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach an isolation circuit controlled by a programmable element which is blown at a wafer test to isolate defective bitlines from a sense amplifier circuit. And the programmable element fits within a predetermined pitch the sense amplifier circuit.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Baum; Aaron M. et al. (US 6590819 B1), Seok; Yong-Sik (US 5255234 A), Proebsting; Robert J. (US 6462998 B1), Kuge; Shigehiro et al. (US 6850454 B2), Sakata; Takeshi (US 6646934 B2), and Nakano; Masaya (US 6519193 B2) disclose programmable circuits to control isolation circuits for isolating bitlines or wordlines from sense amplifier circuits or wordline driver circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

05-05-05

Son L. Mai
Primary Examiner
Art Unit 2827